UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/541,024	06/28/2005	Mamiko Akizuki	28951.5400	4042

27890 7590 09/02/2008

STEPTOE & JOHNSON LLP
1330 CONNECTICUT AVENUE, N.W.
WASHINGTON, DC 20036

EXAMINER	
ALSIP, MICHAEL	
ART UNIT	PAPER NUMBER
2186	

MAIL DATE	DELIVERY MODE
09/02/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/541,024	AKIZUKI ET AL.	
	Examiner	Art Unit	
	MICHAEL ALSIP	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9,10,13-19,34 and 36-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9,10,13-19,34 and 36-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim34 is objected to because of the following informalities: In line 8 of this claim, the word "request" is misspelled "requ4st". Appropriate correction is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 15, 16 and 19** are rejected under 35 U.S.C. 102(b) as being anticipated by Ochiai et al. (US 6,340,973 B1).

3. Consider **claim 15**, Ochiai et al. discloses a memory controller for controlling a memory having a plurality of banks, the memory controller comprising: an arbitration circuit for arbitrating a memory access request from a plurality of blocks for accessing a memory (Fig. 7, Col. 24 lines 55-67 and Col. 25 lines 1-22), **wherein the plurality of blocks comprises a block for making a memory access request, block access data is a data unit comprising a pair of bank access data belonging to different banks, and a memory request is made by a single bank access data from a block permitted to access the memory** (Fig. 28, Col. 1 lines 31-40 and 65-67, Col. 2 lines 1-2, Col. 5 lines 1-6 and 35-40 and Col. 6 lines 45-51, Col. 7 lines 55-67, Col. 8 lines 1-55 and Col. 12 lines 35-38, Ochiai et al. discloses that sets of bank accesses are ordered

and grouped so that consecutive requests are to different banks and split-banks before accesses to the same bank or split-bank, therefore disclosing grouping bank access data so that they are to different banks, this grouping is the same as pairing up, therefore disclosing the concept of pairs)**, the arbitration circuit comprising: a request receiving block for receiving memory requests from the plurality of blocks, the request receiving block comprising a data unit decision unit for deciding whether a data unit of requested memory access based on the received memory request is a data unit comprising two sets of the bank access data or the bank access data alone, and instructing the command generation block to provide a wait cycle when a memory access request is made by the bank access data alone from the block permitted to access the memory** (Ochiai et al.: Fig. 8 and 28, Col. 1 lines 31-40 and 65-67, Col. 2 lines 1-2, Col. 5 lines 1-6 and 35-40 and Col. 6 lines 45-51, Col. 7 lines 55-67, Col. 8 lines 1-55, Col. 12 lines 35-38, Col. 25 lines 23-67, and Col. 26 lines 1-9)**; a wait cycle designating unit for designating the number of wait cycles provided when memory access is requested from the plurality of blocks by the bank access data alone** (Fig. 28, when an idle command is issued, by issuing the command and then issuing the next command some time later, the number of idle cycles is designated)**; an enabling signal generation block which is instructed by the request receiving block for generating the enabling signal and outputting the enabling signal to the block permitted to access the memory** (Ochiai et al.: Col. 24 lines 55-67)**; and a control signal generation block which is instructed by the request receiving block for generating the control signal and**

generates each control signal (Ochiai et al.: Col. 24 lines 55-67)**;** a command generation block for generating a memory command for a memory based on a control signal from the arbitration circuit (Fig. 1, abstract, Col. 5 lines 26-34); an address generation block for receiving a memory address from a block permitted by the arbitration circuit for accessing a memory and outputting the memory address to such memory (Fig. 1, abstract, Col. 2 lines 23-25, Col. 5 lines 20-25 and Col. 6 lines 3-7); and a data latch block for latching either write data from the block permitted by the arbitration circuit for accessing a memory or read data from a memory and passing data between a memory and the block (Fig. 1, abstract, Col. 2 lines 32-36, and Col. 5 31-34).

4. Consider **claim 16,** as applied to **claim 15** above, Ochiai et al. discloses wherein the arbitration circuit comprises: a memory access priority designating unit for designating priority of memory access from the plurality of blocks (Ochiai et al.: Fig. 8, Col. 25 lines 23-67, and Col. 26 lines 1-9).

5. Consider **claim 19,** as applied to **claim 15** above, Ochiai et al. discloses wherein the memory is s synchronous memory (Ochiai et al.: Col. 1 lines 20-29 and Col. 20 line 36).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. **Claims 17 and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochiai et al. (US 6,340,973 B1).

9. Consider **claim 17,** as applied to **claim 16** above, Ochiai et al. does not explicitly state wherein the memory access priority designating unit is set from outside and priority of access from the plurality of blocks to the memory is changed according to a setting of the memory access priority designating unit, however the examiner is taking official notice to the fact that a device being able to accept user input to change device parameters to better suit the user's needs is well known and conventional.

It would have been obvious to one of ordinary skill in the art at the time of the invention to be able to accept user input to change device parameters to better suit the user's needs in the system of Ochiai et al. because, this allows for more system flexibility during various applications and also provides a better user experience.

10. Consider **claim 18,** as applied to **claim 16** above, Ochiai et al. does not explicitly state wherein the wait cycle designating unit is set from outside and the number of wait cycles provided by the command generation block is changed according to a setting of the wait cycle designating unit, however the examiner is taking official notice to the fact

that a device being able to accept user input to change device parameters to better suit the user's needs is well known and conventional.

It would have been obvious to one of ordinary skill in the art at the time of the invention to be able to accept user input to change device parameters to better suit the user's needs in the system of Ochiai et al. because, this allows for more system flexibility during various applications and also provides a better user experience.

11. **Claims 34 and 36-40** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochiai et al. (US 6,340,973 B1), and further in view of Miyawaki et al. (US 5,752,266).

12. Consider **claim 34**, Ochiai et al. discloses a memory controller for controlling a memory having a plurality of banks, the memory controller comprising: an arbitration circuit for arbitrating a memory access request from a plurality of blocks for accessing a memory (Fig. 7, Col. 24 lines 55-67 and Col. 25 lines 1-22), **the arbitration circuit comprises: a bank decision unit for receiving a memory address from the plurality of blocks and deciding whether access is made to the same bank based on the received memory address** (Ochiai et al.: Fig. 8, Col. 25 lines 23-67, and Col. 26 lines 1-9)**, an access request decision unit for receiving a memory request from the plurality of blocks and deciding the kind of requested memory access based on the received memory request** (Ochiai et al.: Fig. 8, Col. 25 lines 23-67, and Col. 26 lines 1-9, Miyawaki et al.: Col. 2 lines 1-67 and Col. 8 lines 61-67)**, a request receiving block comprising the bank decision unit and the access request decision unit and provides an instruction to generate an enabling signal** (Ochiai et al.: Fig. 8, Col. 25

lines 23-67, and Col. 26 lines 1-9 and Miyawaki et al.: Col. 2 lines 1-67 and Col. 8 lines 61-67)**, a memory access priority designating unit for designating the priority of memory access from the plurality of blocks** (Ochiai et al.: Fig. 8, Col. 25 lines 23-67, and Col. 26 lines 1-9)**, an arbitrating method designating unit for designating either higher priority on a bank changing the priority of memory access to prevent successive access to the same bank or higher priority on access changing the priority of memory access to have successive read access when the memory access request from the plurality of blocks is made to the same bank as immediately preceding access and memory access permitted by the arbitration circuit immediately before is read access** (Ochiai et al. Col. 1 lines 65-67, Col. 2 lines 1-2, Col. 5 lines 1-6 and 35-40 and Col. 6 lines 45-51 and Col. 12 lines 35-38) and where Ochiai et al. does not explicitly disclose changing the priority of memory accesses, however Miyawaki et al. does teach this feature: (abstract, Col. 1 line 67, Col. 2 lines 1-5 and Col. 4 lines 33-40)**;**

It would have been obvious to one of ordinary skill in the art at the time of the invention to change the priority of memory access in the system of Ochiai et al. as done in Miyawaki et al. because, Miyawaki et al. teaches that this will thereby avoid concentration on or rejection of a specific memory access operation and eliminating an ineffective period and that the user receives an efficient memory system without increasing the capacity of a buffer memory, the width of a memory bus, or an operating frequency (abstract and Col. 2 lines 3-5).

an identical bank priority designating unit for selecting a block to be subsequently permitted to access when the arbitrating method designating unit is set so as to place higher priority on a bank (Ochiai et al.: Fig. 8, Col. 25 lines 23-67, and Col. 26 lines 1-9), **a read access priority designating unit for selecting a block to be subsequently permitted to perform read access when the arbitrating method designating unit is set so as to place higher priority on access** (Miyawaki et al.: abstract, Col. 1 line 67, Col. 2 lines 1-5 and 34-67 and Col. 4 lines 33-40), **an enabling signal generation block which is instructed by the request receiving block for generating the enabling signal and outputting the enabling signal to the block permitted to access the memory** (Ochiai et al.: Col. 24 lines 55-67), **and a control signal generation block which is instructed by the request receiving block for generating the control signal and generating each control signal** (Ochiai et al.: Col. 24 lines 55-67), a command generation block for generating a memory command for a memory based on a control signal from the arbitration circuit (Fig. 1, abstract, Col. 5 lines 26-34), an address generation block for receiving a memory address from a block permitted by the arbitration circuit for accessing a memory and outputting the memory address to such memory (Fig. 1, abstract, Col. 2 lines 23-25, Col. 5 lines 20-25 and Col. 6 lines 3-7), and a data latch block for latching either write data from the block permitted by the arbitration circuit for accessing a memory or read data from a memory and passing data between a memory and the block (Fig. 1, abstract, Col. 2 lines 32-36, and Col. 5 31-34), as for the limitation:

13. Consider **claim 36,** as applied to **claim 34** above, Ochiai et al. in view of Miyawaki et al. does not directly disclose wherein the memory access priority designating unit is set from outside and the priority of access from the plurality of blocks to the memory is changed according to a setting of the memory access priority designating unit, however the examiner is taking official notice to the fact that a device being able to accept user input to change device parameters to better suit the user's needs is well known and conventional.

It would have been obvious to one of ordinary skill in the art at the time of the invention to be able to accept user input to change device parameters to better suit the user's needs in the system of Ochiai et al. in view of Miyawaki because, this allows for more system flexibility during various applications and also provides a better user experience.

14. Consider **claim 37,** as applied to **claim 35** above, Ochiai et al. in view of Miyawaki et al. does not directly disclose wherein the arbitrating method designating unit is set from outside and the arbitrating method of memory access from the plurality of blocks is changed according to a setting of the arbitrating method designating unit, however the examiner is taking official notice to the fact that a device being able to accept user input to change device parameters to better suit the user's needs is well known and conventional.

It would have been obvious to one of ordinary skill in the art at the time of the invention to be able to accept user input to change device parameters to better suit the user's needs in the system of Ochiai et al. in view of Miyawaki because, this allows for

more system flexibility during various applications and also provides a better user experience.

15. Consider **claim 38,** as applied to **claim 35** above, Ochiai et al. in view of Miyawaki et al. does not directly disclose wherein the identical bank priority designating unit is set from outside and a block to be subsequently permitted to access to the memory is selected according to priority set by the identical bank priority designating unit when the arbitrating method designating unit is set so as to place higher priority on a bank and a memory access request is made from the plurality of blocks to the same bank as immediately preceding access, however the examiner is taking official notice to the fact that a device being able to accept user input to change device parameters to better suit the user's needs is well known and conventional.

It would have been obvious to one of ordinary skill in the art at the time of the invention to be able to accept user input to change device parameters to better suit the user's needs in the system of Ochiai et al. in view of Miyawaki because, this allows for more system flexibility during various applications and also provides a better user experience.

16. Consider **claim 39,** as applied to **claim 35** above, Ochiai et al. in view of Miyawaki et al. does not directly disclose wherein the read access priority designating unit is set from outside and a block to be subsequently permitted to perform read access to the memory is selected according to priority set by the read access priority designating unit when the arbitrating method designating unit is set so as to place higher priority on access and memory access permitted by the arbitration circuit

immediately before is read access, however the examiner is taking official notice to the fact that a device being able to accept user input to change device parameters to better suit the user's needs is well known and conventional.

It would have been obvious to one of ordinary skill in the art at the time of the invention to be able to accept user input to change device parameters to better suit the user's needs in the system of Ochiai et al. in view of Miyawaki because, this allows for more system flexibility during various applications and also provides a better user experience.

17. Consider **claim 40,** as applied to **claim 34** above, Ochiai et al. in view of Miyawaki et al. disclose wherein the memory is s synchronous memory (Ochiai et al.: Col. 1 lines 20-29 and Col. 20 line 36).

18. **Claims 9, 10, 13-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochiai et al. (US 6,340,973 B1) in view of Miyawaki et al. (US 5,752,266) as applied to **claim 9** above, and further in view of Talbot et al. (US 6,976,135 B1).

Consider **claim 9**, Ochiai et al. discloses a memory controller for controlling a memory having a plurality of banks, the memory controller comprising: an arbitration circuit for arbitrating a memory access request from a plurality of blocks for accessing a memory (Fig. 7, Col. 24 lines 55-67 and Col. 25 lines 1-22); **wherein bank access data is access data to the memory, with a predetermined number of bytes for writing or reading on the same bank of the memory and block access data is a data unit with a pair of bank access data including a first-half bank access data and a second-half bank access data belonging to different banks, the arbitration circuit**

comprising (Col. 1 lines 31-40 and 65-67, Col. 2 lines 1-2, Col. 5 lines 1-6 and 35-40 and Col. 6 lines 45-51, Col. 7 lines 55-67, Col. 8 lines 1-55 and Col. 12 lines 35-38, Ochiai et al. discloses that sets of bank accesses are ordered and grouped so that consecutive requests are to different banks and split-banks before accesses to the same bank or split-bank, therefore disclosing grouping bank access data so that they are to different banks, this grouping is the same as pairing up, therefore disclosing the concept of pairs), **a request receiving block for receiving a block access data and determining a change in an order of memory access if a second-half bank access data of a block access data where memory access is permitted immediately before is the same as a first-half bank access data of a block access data of a subsequent memory access request** (Ochiai et al.: Fig. 8, Col. 7 lines 55-67, Col. 8 lines 1-23, Col. 25 lines 23-67, and Col. 26 lines 1-9), where Ochiai et al. discloses an ordering and optimization of this ordering and reverse ordering, that will have consecutive requests to different banks and split-banks before consecutive requests to the same banks or split-banks, but Ochiai et al. does not directly state that an established order is changed, whereas Miyawaki et al. does teach this feature: abstract, Col. 1 line 67, Col. 2 lines 1-5 and Col. 4 lines 33-40).

It would have been obvious to one of ordinary skill in the art at the time of the invention to change the priority of memory access in the system of Ochiai et al. as done in Miyawaki et al. because, Miyawaki et al. teaches that this will thereby avoid concentration on or rejection of a specific memory access operation and eliminating an ineffective period and that the user receives an efficient memory system without

increasing the capacity of a buffer memory, the width of a memory bus, or an operating frequency (abstract and Col. 2 lines 3-5).

an enabling signal generation block which is instructed by the request receiving block for generating an enabling signal and outputting the enabling signal to the block permitted to access the memory (Ochiai et al.: Col. 24 lines 55-67), and a control signal generation block which is instructed by the request receiving block for generating the control signal (Ochiai et al.: Col. 24 lines 55-67);

a command generation block for generating **a** memory command for **the** memory based on **the** control signal from the arbitration circuit (Fig. 1, abstract, Col. 5 lines 26-34), an address generation block for receiving a memory address from a block permitted to access by the arbitration circuit and for outputting the memory address to the memory (Fig. 1, abstract, Col. 2 lines 23-25, Col. 5 lines 20-25 and Col. 6 lines 3-7), and a data latch block for latching either write data from the block permitted by the arbitration circuit for accessing a memory or read data from a memory and passing data between a memory and the block (Fig. 1, abstract, Col. 2 lines 32-36, and Col. 5 31-34),

Ochiai et al. in view of Miyawaki et al. also disclose wherein the data latch block comprises: **a write data latch block for receiving and latching write data from the plurality of blocks** (Ochiai et al.: Fig. 1, abstract, Col. 2 lines 32-36, and Col. 5 31-34), **a read data latch block for receiving and latching the read data having been read from the memory** (Ochiai et al.: Fig. 1, abstract, Col. 2 lines 32-36, and Col. 5 31-34), as for the limitations: **a data change block for either changing an order of bank**

access data outputted by the write data latch block and outputting data as write data to the memory, or changing an order of bank access data outputted by a read data latch block and outputting data as read data to a block permitted to perform read access to the memory, wherein the data change block is controlled based on a data latch control signal from the arbitration circuit indicating a change in the order of memory access of the first-half and second-half bank access data in the block access data. (Ochiai et al.: Col. 2 lines 33-36 and Col. 5 lines 31-35) where Ochiai et al. describes the data processor transferring and mediating the data but does not explicitly state reordering the data, whereas Talbot et al. does teach this feature (Fig. 4, abstract, Col. 5 lines 6-34).

It would have been obvious to one of ordinary skill in the art at the time of the invention to reorder the bank access data in the data latch block in the system of Ochiai et al. in view of Miyawaki et al. because Talbot et al. teaches that doing so bandwidth is maximized and concurrency is maximized by minimizing the amount of time that memory requests must wait to be serviced (Col. 2 lines 6-31).

19. Consider **claim 10,** as applied to **claim 9** above, Ochiai et al. in view of Miyawaki et al. and Talbot et al. disclose wherein the arbitration circuit comprises: a memory access priority designating unit for designating priority of memory access from the plurality of blocks. (Ochiai et al.: Fig. 8, Col. 25 lines 23-67, and Col. 26 lines 1-9),

20. Consider **claim 13,** as applied to **claim 10** above, Ochiai et al. in view of Miyawaki et al. do not explicitly state wherein the memory access priority designating unit is set from outside and the priority of access from the plurality of blocks to the

memory is changed according to a setting of the memory access priority designating unit, however the examiner is taking official notice to the fact that a device being able to accept user input to change device parameters to better suit the user's needs is well known and conventional.

It would have been obvious to one of ordinary skill in the art at the time of the invention to be able to accept user input to change device parameters to better suit the user's needs in the system of Ochiai et al. in view of Miyawaki because, this allows for more system flexibility during various applications and also provides a better user experience.

21. Consider **claim 14,** as applied to **claim 9** above, Ochiai et al. in view of Miyawaki et al. disclose wherein the memory is s synchronous memory (Ochiai et al.: Col. 1 lines 20-29 and Col. 20 line 36).

Response to Arguments

22. Applicant's arguments filed 6/30/2008 have been fully considered but they are not persuasive. The arguments pertaining to the newly amended claim language are addressed in the claims themselves.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL ALSIP whose telephone number is (571)270-1182. The examiner can normally be reached on Monday through Friday 7:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Matt Kim/
Supervisory Patent Examiner, Art Unit 2186

Michael Alsip
Examiner
Art Unit 2186

/Michael Alsip/
Examiner, Art Unit 2186

August 27, 2008